IN THE CLAIMS:

Please amend the claims as follows. The claims are in the format as required by 35 C.F.R. § 1.121.

1. (Currently Amended) A method comprising:

receiving one or more bits of synchronization data from a transmitter in a receiver of a communications link;

loading the one or more bits of synchronization data into a shift register in the receiver, wherein the receiver shift register has a feedback circuit;

if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with a corresponding transmitter shift register, wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors such that the integrity of the communications link can be continually monitored; and

if the receiver shift register is not filled with synchronization data, shifting the loaded synchronization data and loading one or more additional bits of synchronization data into the receiver shift register.

2. (Original) The method of claim 1, wherein receiving one or more bits of synchronization data comprises receiving idle codes containing synchronization data.

3. (Original) The method of claim 1, further comprising determining whether the receiver shift register is filled with synchronization data by counting a predetermined number of cycles after a reset event.

4. (Original) The method of claim 1, wherein the receiver shift register comprises a plurality of serially coupled flip-flops, and wherein shifting the loaded synchronization data comprises shifting the bit in each flip-flop to a next flip-flop.

5. (Original) The method of claim 1, wherein loading the one or more additional bits of synchronization data into the receiver shift register comprises loading the one or more additional bits of synchronization data into one or more predetermined cells of the receiver shift register.

6. Cancelled.

7. (Currently Amended) A system comprising:

a receiver shift register; and

a feedback circuit coupled to the receiver shift register;

wherein one or more cells of the receiver shift register are configured to alternatively accept as input either a bit from a preceding cell or a received bit of synchronization data from a transmitter, and

wherein if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with a corresponding transmitter shift register, wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors such that the integrity of the communications link can be continually monitored.

8. (Currently Amended) The system of claim 7, further comprising a counter coupled to the receiver shift register, wherein the counter is configured to assert a "synchronized" signal when a predetermined count is reached after a reset event.

9. (Currently Amended) The system of claim 8, wherein the predetermined count corresponds to the receiver shift register being filled with synchronization data.

10. (Currently Amended) The system of claim 7, wherein the one or more cells of the receiver shift register are configured to accept received bits of synchronization data as input until the receiver shift register is filled with synchronization data, and to accept bits from preceding cells as input when the receiver shift register is filled with synchronization data.

11. (Currently Amended) The system of claim 7, wherein upon occurrence of a reset event, data in the receiver shift register is invalid data.

12. (Original) The system of claim 7, further comprising one or more demultiplexers coupled to provide input to the one or more cells, wherein the one or more demultiplexers are configured to select either bits from preceding cells or received bits of synchronization data to provide as input to the one or more cells.

13. (Original) The system of claim 12, wherein the demultiplexers are coupled to receive an indication of whether the receiver shift register is synchronized.

14. (Original) The system of claim 13, wherein the demultiplexers are coupled to a counter, wherein the counter is configured to provide the indication when a predetermined count is reached after a reset event.

15. (Original) The system of claim 7, further comprising a transmission medium coupled to the receiver shift register.

16. (Original) The system of claim 15, wherein the transmission medium is configured to transport the synchronization data in idle codes.

17. (Currently Amended) The system of claim 7, ~~further comprising a~~ wherein the transmitter shift register ~~which~~ is configured to generate a first bit sequence, ~~wherein~~ and the receiver shift register is configured to generate an identical bit sequence.

18. Cancelled.

19. (Original) The system of claim 7, wherein the receiver shift register is configured to load synchronization data on each cycle into one or more predetermined cells of the receiver shift register.

20. (Original) The system of claim 19, wherein the one or more predetermined cells of the receiver shift register exclude at least one of the cells of the receiver shift register.

21. (Original) The system of claim 20, wherein the receiver shift register cells comprise 11 serially coupled flip-flops and wherein the predetermined cells comprise 8 consecutive ones of the 11 serially coupled flip-flops.

22. (Original) The system of claim 7, wherein the feedback circuit comprises an exclusive OR (XOR) gate having two inputs coupled to receive the outputs of two of the cells of the receiver shift register, the XOR gate further having an output that is coupled to the input of a first cell of the receiver shift register.

23. (Currently Amended) A system comprising:

a receiver shift register; and

a feedback circuit coupled to the receiver shift register;

wherein one or more cells of the receiver shift register are configured to initially alternatively accept as input a received bit of synchronization data from a transmitter and, upon receiving an indication that the receiver shift register is synchronized with the transmitter, accept as input a bit from a preceding cell, and

wherein if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with a corresponding transmitter shift register, wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors such that the integrity of the communications link can be continually monitored.